WHAT IS CLAIMED IS:

1. A fast Fourier transform (FFT) architecture, comprising:

a pipeline segment having a plurality of data-independent pipelines that receive different time-domain data samples and generate therefrom corresponding intermediate results; and

a parallel segment, coupled to all of said pipelines, that receives said corresponding intermediate results and generates therefrom corresponding frequency-domain results.

2. The architecture as recited in Claim 1 wherein each of said plurality of data-independent pipelines receives a single time-domain data sample at a time.

3. The architecture as recited in Claim 1 wherein each of said data-independent pipelines is a radix-2^2 single-path delay feedback pipeline.

4. The architecture as recited in Claim 1 wherein said parallel segment is a radix-2 segment.

5. The architecture as recited in Claim 1 wherein a number of said plurality of data-independent pipelines for a particular application is based on both a time-domain data sample rate and a clock rate pertaining to said application.

6. The architecture as recited in Claim 1 wherein a strength reduction transformation is employed to substitute real multipliers for complex multipliers.

7. The architecture as recited in Claim 1 wherein said pipeline segment employs a hardware implementation.

8. A method of performing a fast Fourier transform (FFT), comprising:

initially receiving different time-domain data samples into a plurality of data-independent pipelines of a pipeline segment, said data-independent pipelines generating therefrom corresponding intermediate results; and

subsequently receiving said corresponding intermediate results into a parallel segment coupled to all of said pipelines, said parallel segment generating therefrom corresponding frequency-domain results.

9. The method as recited in Claim 8 wherein each of said plurality of data-independent pipelines receives a single time-domain data sample at a time.

10. The method as recited in Claim 8 wherein each of said data-independent pipelines is a radix-2^2 single-path delay feedback pipeline.

11. The method as recited in Claim 8 wherein said parallel segment is a radix-2 segment.

12. The method as recited in Claim 8 wherein a number of said plurality of data-independent pipelines for a particular application is based on both a time-domain data sample rate and a clock rate pertaining to said application.

13. The method as recited in Claim 8 wherein a strength reduction transformation is employed to substitute real multipliers for complex multipliers.

14. The method as recited in Claim 8 wherein said pipeline segment employs a hardware implementation.

15. An Orthogonal Frequency Division Multiplex (OFDM) receiver, comprising:

an input section that is coupled to a receive antenna;

a fast Fourier transform (FFT) section that is coupled to said receive section, including:

a pipeline segment having a plurality of data-independent pipelines that receive different time-domain data samples and generate therefrom corresponding intermediate results, and

a parallel segment, coupled to all of said pipelines, that receives said corresponding intermediate results and generates therefrom corresponding frequency-domain results; and

an output section that is coupled to said FFT section.

16. The receiver as recited in Claim 15 wherein each of said plurality of data-independent pipelines receives a single time-domain data sample at a time.

17. The receiver as recited in Claim 15 wherein each of said data-independent pipelines is a radix-2^2 single-path delay feedback pipeline.

18. The receiver as recited in Claim 15 wherein said parallel segment is a radix-2 segment.

19. The receiver as recited in Claim 15 wherein a number of said plurality of data-independent pipelines for a particular application is based on both a time-domain data sample rate and a clock rate pertaining to said application.

20. The receiver as recited in Claim 15 wherein a strength reduction transformation is employed to substitute real multipliers for complex multipliers.

21. The receiver as recited in Claim 15 wherein said pipeline segment employs a hardware implementation.